

Parallel Processing Solves the DTV Format Conversion Problem

Jed Deame
Director of Product Development
TeraNex, Inc.
Orlando, Florida

Abstract

The FCC mandate to broadcast Digital Television (DTV) has forced broadcasters to face the challenge of integrating High Definition Television (HDTV) programming into their NTSC or 601 plants. In the early stages of the DTV rollout, broadcasters will be required to simultaneously broadcast program material on both digital and analog channels (simulcast). In addition, broadcasters will need to combine locally generated advertising, programming and logos with network generated programming. However, this material will now be in a variety of different high definition and standard definition formats. This will force the broadcaster to convert most of their material from standard definition to high definition (up-convert), from high definition to standard definition (down-convert), or from one high definition format to another (side-convert). Often all of these conversions will need to be performed simultaneously. This has created an instant need for a variety of format converters.

The typical approach to format conversion is to “hard-wire” the processing algorithms using Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs). This approach has several disadvantages such as limited adaptability to new formats and lack of expandability to higher complexity processing algorithms. This paper describes an alternative approach using massively parallel computer technology to create a fully programmable video processor. This “Video Computer” can be programmed to perform a variety of video processing functions and provides the flexibility and scalability to support emerging formats and expanded capabilities without requiring a system redesign.

Introduction

There is currently a lack of standardization between television networks on a common DTV distribution and transmission format. NBC and CBS have adopted the 1080-line interlaced format whereas ABC and Fox prefer the progressive formats. The Direct Satellite broadcasters have chosen their own custom formats as most likely will the cable

operators. Broadcasters will choose their preferred formats based on program content, multicast requirements, interactivity requirements, compatibility with existing infrastructure, and other factors. Small changes to the picture size and frame rate can free up significant bandwidth for other non-video data, such as Internet or e-commerce. While the current generation of DTV up/down converters support most of the popular 30fps interlaced and 60fps progressive formats, the equipment manufacturers have been slow to support emerging formats such as 480p30, 480p60 and 1080p24. This makes the decision of when to commit to a fixed function format converter a daunting task for the affiliates and post houses.

If dealing with a variety of current and emerging formats is inevitable, how can the broadcaster or post house justify an investment in format converters which may be obsolete within a year or two? Ideally, they would select a unit that not only supports all the existing formats, but also can be field upgraded to support any emerging formats as they are defined. Unfortunately, none of the current converter manufacturers offer such a "future proof" solution. This is because they implement their solutions in hard-wired ASICs and FPGAs, which cannot be reprogrammed to support emerging standards. The ideal solution would be a fully programmable solution, which could be programmed to support any desired format. Unfortunately, conventional microprocessors are not up to the task of broadcast quality format conversion.

Video Processing Requirements

Multimedia data, especially video data, is fundamentally different from non-media application data because it is comprised of a series of related data points derived from sampling analog signals over time. The sampled analog signals of multimedia data are the visual images and the sounds of the real world. Over 350,000 sample data points (pixels) are required to represent just a single standard definition television (SDTV) frame. At thirty frames per second and twenty bits per pixel (average), this corresponds to a data rate of over 26 Megabytes per second. The emerging High Definition Television (HDTV) pictures contain nearly six times the number of pixels of today's TV images, generating a data stream of over 155 Megabytes per second.

Video processing is highly computationally demanding not only because of the huge amount of data that must be processed in an individual image, but also because it requires real-time response (computations). Video processing requires 100's, even 1000's of operations per data sample, which together with the very high data rates necessitated by real-time processing, combine to require 10's, even 100's of billions of operations per second (BOPS, or giga-ops, GOPS).

Effective video processing requires more than 100 times the computer processing power offered by traditional processors. Media operations on the fastest PC's and workstations often require a minute or more, when only a 1/30 of a second is available for real-time operation. Media data processing is also different because the limits of human perception allow a much lower precision representation of images and sounds (i.e., 8-10

bits/sample for video data compared to 32-64 bits/sample for business and scientific data and computations).

Competitive Architecture Shortcomings

Video Processing efficiency and scalability cannot be achieved without exploitation of the unique characteristics and needs of image processing applications, data structures, and algorithms. Traditional control processor (e.g., Pentium, PowerPC, SPARC, etc.) and even more recent Digital Signal Processor (i.e., “DSP,” including the C80, i860, SHARC) architectures were each designed for efficient processing in their respective domains. However, neither achieves high efficiency when applied to advanced image processing applications. “Hard-wired” FPGA or ASIC based approaches designed for specific data processing problems achieve good efficiency for their intended applications; however, they lack both scalability and applicability to other image processing applications, even when considerable similarity exists. Programmable architectures are required in order to benefit from algorithm advances with a minimum life cycle cost impact.

Parallel Processing Approach

A massively parallel array of processors can easily handle the processing load of video processing applications such as format conversion, with capacity to spare, to solve future format conversion problems. In addition, the tremendous processing power available would provide a practical way to implement advanced techniques such as motion compensation – the same technology that makes high-end standards converters look so good. With a programmable solution, the problem of format conversion now becomes a software task, enabling very fast development cycles as well as continuously improved picture quality through processing algorithm enhancements. In comparison, current format converter solutions must commit the algorithms to silicon early in the development cycle and have no provision for functional or quality upgrades.

Parallel processing solves the associated problems of format conversion by implementing the highly compute intensive motion compensation algorithms and providing for rapid support of the continuously changing image format standards. A unique computing architecture, specifically designed for processing of video and infrared imagery in the most cost effective and efficient manner, has been developed by Lockheed Martin. This technology, when applied to the format conversion problem, provides a practical way to solve the problems associated with format conversion.

The GAPP Processor

Over the last fifteen years, Lockheed Martin Electronics & Missiles, a major defense contractor, has made a substantial investment in developing parallel processing architectures for ultra high-speed image processing. The majority of this work was

funded by the DOD, which was motivated by the unique military need for performing pattern recognition (for targeting) on multiple high speed video data streams, within minimum military platform physical constraints (i.e., size, weight and power). These requirements resulted in the revolutionary development of the Geometric Arithmetic Parallel Processor (**GAPP**), a fine-grained, massively parallel, two dimensional mesh computer architecture that is uniquely efficient for two dimensional, video processing applications.

Lockheed Martin, with government sponsorship, has invested over \$100 Million to develop, apply and refine the GAPP architecture for solving complex, video rate image processing applications. GAPP, a Single-Instruction-Multiple Data (SIMD) massively parallel and scalable architecture, was invented in response to the absence of a computing architecture that provides comparable video processing throughput, scalability and flexibility. In 1998, the GAPP architecture was migrated to a 0.25 micron VLSI chip that allows scalable video processors with from one thousand to one million compute engines (i.e., one chip to 32 x 32 chips) to be controlled with identical software. Four patents have been issued and eight are pending.

Lockheed Martin is not the only company that has embraced the SIMD architecture to solve compute intensive problems. Computers built by Cray, Connection Machines, and MasPar have proven the viability of the SIMD architecture, but at enormous cost. By utilizing the latest chip fabrication techniques and years of design effort at Lockheed Martin, the TeraNex GAPP chip can be manufactured quite inexpensively, yet outperform computers costing millions of dollars just a few years ago.

Sun, Intel and Motorola in the past few years have started to manufacture primitive SIMD computers for demanding image and data processing applications. Intel now uses MMX (a SIMD architecture) in their processors and Motorola is now selling the AltiVec chip (a SIMD architecture) as a co-processor on the Power PC for demanding image and other data processing applications. The GAPP is several generations ahead of these products relative to processing power, capability and, most importantly, software support. TeraNex's processors are now in their sixth generation. They are highly refined, field proven, and reliable.

GAPP Architecture Overview

Technically, GAPP is a massively parallel super-computer organized in a two-dimensional Single Instruction Multiple Data (SIMD) architecture. Effectively, this is a collection of thousands of RISC type computers operating in unison. The computers, called Processing Elements (PE's), are arranged in a two dimensional grid – each PE linked to the four PE's closest to it in the grid. Each PE has its own data memory, and all PE's run the same program simultaneously. In the latest generation of GAPP, there are 1024 PE's on each chip – arranged in a grid 32 PE's wide by 32 PE's high. Running at a clock speed of 90 MHz, each chip can execute over 90 billion operations per second (BOPS). Furthermore, the architecture is fully scalable - the chips can be combined in

two-dimensional arrays to build computers with over 1 million PE's, yielding computing performance measured in trillions of operations per second (TeraOPs).

While capable of enormous processing power, computers built to the SIMD architecture are highly specialized in function. SIMD works well on problems that require large amounts of data to be processed in exactly the same way. GAPP in particular is ideally suited to perform digital image processing.

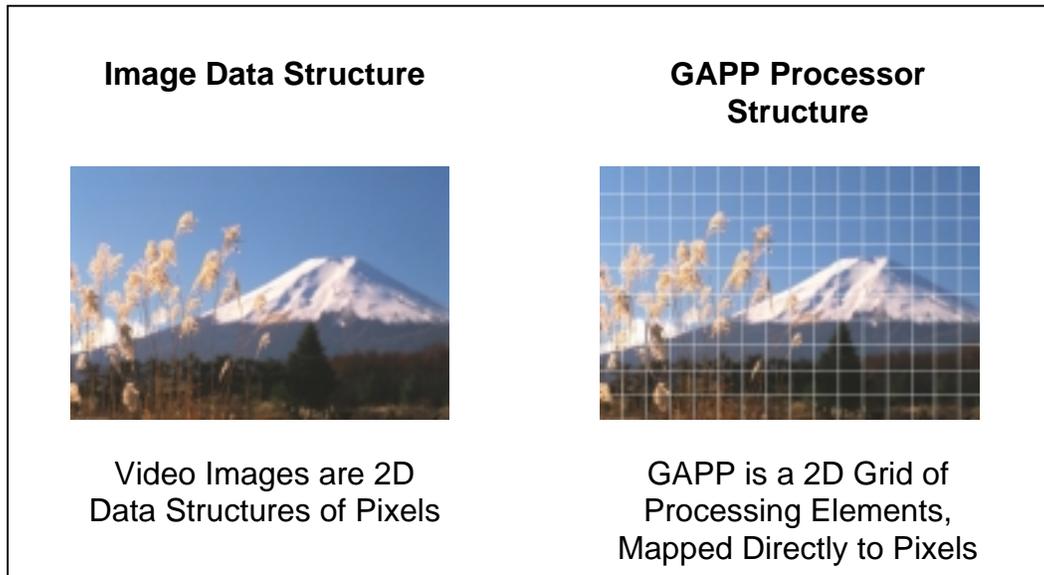


Figure 1: The GAPP Architecture Exploits the Grid Data Structure of Images

As shown in Figure 1, a digital image is a two-dimensional array of data points, or pixels, each describing the brightness and color of a spot on the image. A SIMD "Video Computer" can enhance an image or extract information from it by storing the pixels in memory and performing computations on them in parallel. Some image processing functions, called *point operators*, work on a single pixel regardless of its position in the image. However, pixels are like pieces of a puzzle – they contain valuable information themselves but how they fit together with the pieces around them is often more important. The majority of image processing functions, called *neighborhood operators*, process a group of neighboring pixels in each operation. Neighborhood operations are where GAPP stands out. The two-dimensional architecture mirrors the layout of pixels in an image: each PE has access to its neighbor's memory, allowing it to perform neighborhood operations as easily as point operations. Furthermore, the GAPP has built-in instructions to perform common neighborhood operations as easily as a Pentium or SPARC processor can add two numbers.

GAPP's two-dimensional SIMD image processing architecture mirrors the two-dimensional data structure of images. It achieves maximum inter-processor communication efficiency with direct nearest neighbor (i.e., north, south, east, west) PE connections, as shown in Figure 2, to form a fine-grained, pixel-to-processor mapping between the computer architecture and the image data structure.

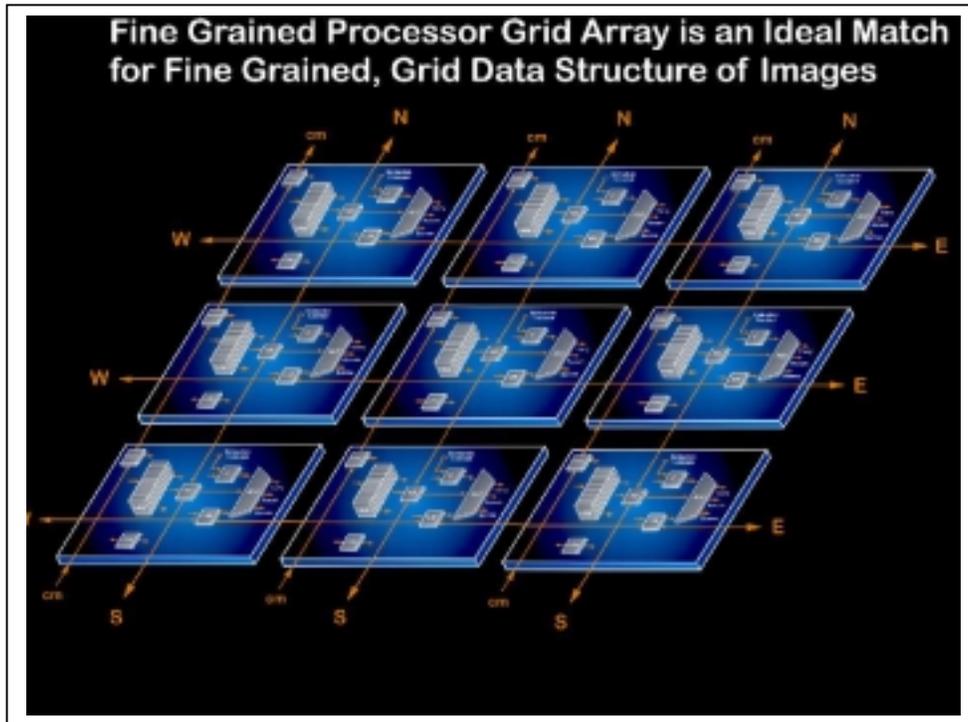


Figure 2: Inter-Processor Communication

The bit-serial design of the GAPP architecture represents the logical extension of the reduced instruction set computer (RISC) design concept. When required by the algorithm suite, the SIMD bit-serial processing element (PE) is flexible enough to perform 1 bit or full precision floating point operations. In all cases, there is no excess hardware to be idled during lower precision operations. This is not the case when DSP computer architectures are used for image processing. GAPP's bit-serial hardware approach yields the highest possible implementation efficiencies.

The two-dimensional grid design of interconnected PEs provides this architecture with inherent scalability. As the processing array is increased in size, all processing resources including the data bandwidth of the inter-PE communications bus (i.e., the two-dimensional processor interconnect grid), processor RAM, and computational throughput increases linearly. To best match the needs of a particular application, the GAPP array size may be scaled to provide the best computational and I/O bandwidth for the application's specific algorithm complexity and processing rate requirements.

GAPP's Technical Superiority

Digital images contain enormous amounts of information. A SMPTE 125M NTSC image is 720 pixels wide by 485 pixels high, almost 350,000 pixels. With 20 bits per pixel (on average) and 30 frames per second, data rates exceed 26 megabytes of data per second. An HDTV image at two megapixels has data rates exceeding 155 megabytes per second. The simple task of moving all this information between the processor and memory can slow a standard computer to a crawl. GAPP has highly optimized, patented circuitry to minimize this overhead and because each PE has its own memory, large portions of the image can be processed completely before being moved – minimizing the number of times the information is moved on and off the chip. GAPP processors achieve their speed by naturally exploiting the two dimensional, low data precision nature of video images, resulting in a processor that is hundreds of times more efficient for performing video processing.

The GAPP architecture is technically superior to FPGAs, ASICs, and DSPs for processing video data because of a combination of four features: arithmetic efficiency, arithmetic scalability, local communication efficiency and high speed I/O. First, the GAPP is arithmetically efficient in that it automatically configures itself to the resolution of the data. The lower the data resolution, the faster the processing. For example, processing 10-bit data takes exactly 25% more processing power than processing 8-bit data. In contrast, conventional processors must pad the data to 16-bits, requiring double the processing power.

Second, the GAPP is arithmetically scalable, in that as the processing power requirement increases, additional GAPPs can be added with virtually no changes to the supporting software. Scalability allows optimization of the number of compute engines to the overall processing requirements, which in turn is a function of the amount of data (i.e., the video rate standard) and processing requirements (i.e., the product features offered).

Third, the GAPP performs local communication efficiently. Data is moved between the processors and memory via three 1024-bit wide data busses in a single clock cycle (33 gigabytes/second per chip). Data is moved between neighboring chips at a rate of 720 megabytes/second per chip. This high I/O bandwidth is ideally suited to processing video data, which often has dependencies among neighboring pixels.

Last, and perhaps most important, one GAPP VI chip can perform external I/O data transfers at a rate of 720 megabytes per second. An array of 25 chips can sustain an external I/O rate of 3.6 Gigabytes per second. This is over 10 times the data rate of the highest resolution HDTV signal (1080p60).

TeraNex Video Computer Solution

The combination of GAPP technology and world class image processing algorithms allows TeraNex to establish a new cost, performance and feature standard within video processing applications. The GAPP hardware attributes are ideally suited to applications requiring real-time comparisons of complex data patterns as is required in Digital Television Processing. Moreover, the arithmetic scalability of the GAPP enables the development of a full product line of video converters/processors ranging in function and processing power.

TeraNex's initial product offering is a product called the TeraNex Video Computer. The Video Computer may be configured to perform, for example, up-conversion and down-conversion between SDTV and HDTV formats as well as conversion between the standard 18 DTV formats. The TeraNex Video Computer can also be configured to perform compression pre and post processing to improve the end-to-end picture quality of any compressed digital video transmission system.

DTV System Solutions

The HDTV Up-converter (a configuration of the TeraNex Video Computer) is an essential element in an HDTV Television station. A typical application, as diagrammed in Figure 3 below, begins with the collection of SDTV source video. The source video may come from satellite feed, archival videotape, or live studio feed.

Up-Conversion Application

- Network HDTV Pass-through with Local SDTV or HDTV Program Insertion

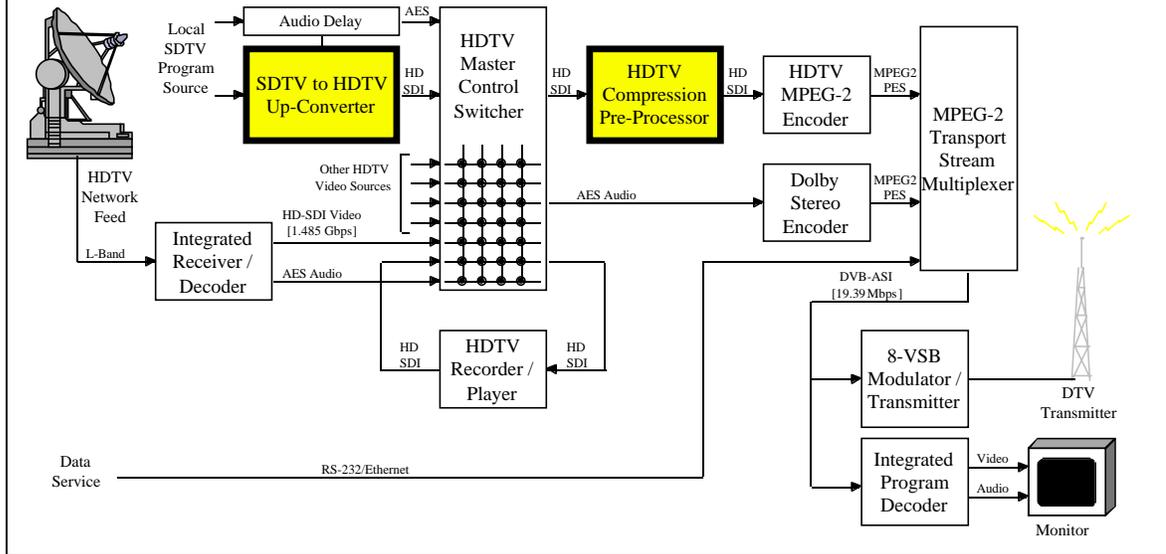


Figure 3: Up-Conversion Application

The SDTV source is converted to the internal HDTV format by the Up-converter and fed to an HDTV switcher where it is mixed with HDTV source material to produce the HDTV master feed. This master feed is then fed to a Compression Pre-Processor (another TeraNex Video Computer) where the data is prepared for MPEG-2 encoding. The final stage of the HDTV processing is MPEG encoding, the process of compressing the 1.24 Gbit digital data stream into the 19.39 Mbit Transport Stream and then 8-VSB modulating to fit within the 6 MHz bandwidth of a single television channel.

Certain broadcasters may choose to down-convert the HDTV network feed so they can take advantage of their SDI plants for processing and local program or graphic insertion. In this case, a Down-converter (a TeraNex Video Computer) may be used for conversion of the HDTV satellite feed to SDTV. After processing the video in the SDTV plant the video is Up-converted (with a second TeraNex Video Computer), conditioned by a Compression Pre-Processor (another TeraNex Video Computer), MPEG encoded, modulated, and transmitted. This process is diagrammed in Figure 4.

Down-Conversion Application

- HDTV Down-Conversion, Local Program or Graphic Insertion, and Up-Conversion

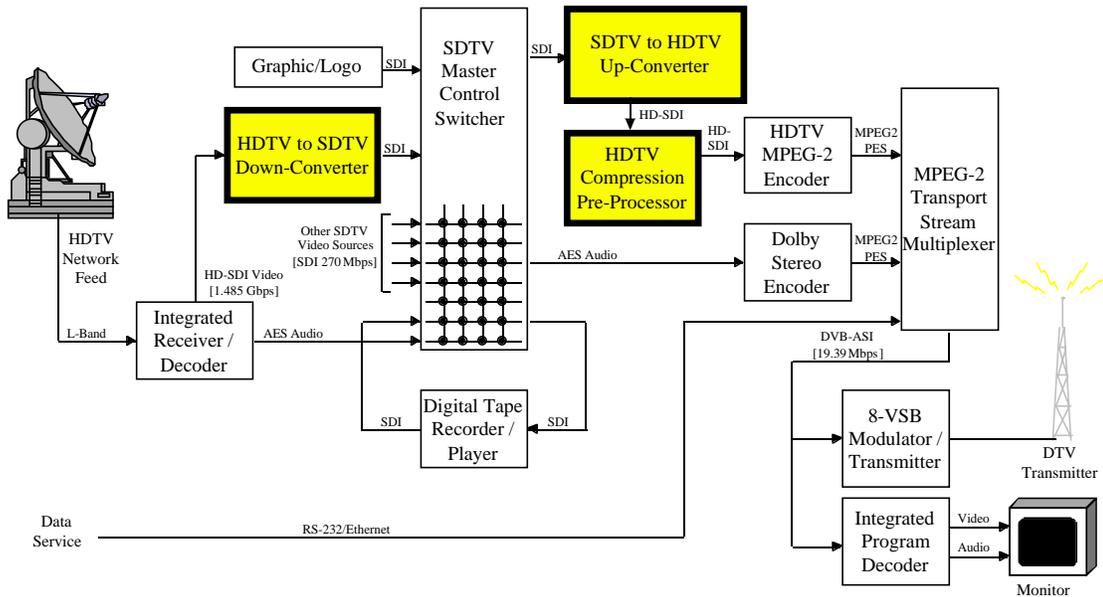


Figure 4: Down-Conversion Application

In Post-Production facilities, the internal HDTV format used may not be the same HDTV format desired by the customer. A TeraNex Video Computer (configured as a Side-Converter) can be used for conversion to and from the plant native HDTV format.

Video Computer Product Overview

The TeraNex Video Computer supports the emerging 24 frame per second HDTV video production standard (1080p24), and its high bandwidth I/O supports conversion between the competing HDTV standards themselves. The additional I/O and processing throughput also supports compression pre and post processing at HDTV resolutions. This ensures that the picture can be processed by the broadcast delivery system without significant degradation due to the 60:1 compression-decompression process mandated by the Standards Committees. Additionally, the improved processing power of the system enables implementation of advanced algorithms for frame rate conversion to support the overseas 50 Hz television systems.

The Video Computer is packaged in a 19" rack mount chassis (6RU high). The I/O supports both SMPTE 259M SDI and SMPTE 292M HD-SDI inputs and outputs with options for 480p60 and analog formats. The Video Computer has the ability to perform all conversions at a level of quality that far exceeds the capabilities of any competitive unit. In addition, the surplus processing power and empty slots provide for system upgrades and feature expansion.

For example, the television and film industry recoups the cost of equipment by direct-use billing hours; this can be accelerated by incrementally adding functionality to a product. Accordingly, there are multiple upgrades, which can be added to the TeraNex Video Computer. For software upgrades, the customer may download code via Ethernet or modem and provide instant product enhancements. Hardware upgrades can be shipped overnight and installed by the customer if desired.

Conclusion

The Video Industry's transition from analog to digital has prompted a new paradigm for video processing. The traditional video "signal" has been replaced by video "data", which enables sophisticated processing functions to be applied to that data. Ultimately, the final quality of the video stream is dependent on the refinement of the image processing algorithms that are applied to it. The TeraNex Video Computer, utilizing advanced SIMD computer technology, enables a high degree of flexibility and scalability to handle many video processing and conversion functions with the highest possible quality. This "future proof" technology enables the broadcaster and post production house to adapt to emerging standards and processing requirements without discarding their initial equipment investment.

The TeraNex Video Computer is capable of meeting the current needs of broadcasters, large post-production houses and duplication facilities. It provides real-time video conversion and a long series of upgrade paths, enabling field upgrades (software and additional boards) to meet the ever-changing needs of the broadcast industry.